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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAVID R. WELLAND,
DONALD A. KERTH, and CAIYI WANG

Appeal 2008-5646
Application 09/686,072
Technology Center 2800

Decided:[1] February 2, 2009

Before KENNETH W. HAIRSTON, JOSEPH F. RUGGIERO,
and KARL D. EASTHOM, *Administrative Patent Judges*.

RUGGIERO, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Final Rejection of claims 1, 3, 4, 52-54, 66-79, and 81-85. Claims 2 and 80 have been canceled, and claims 5-51 and 55-65 have been withdrawn from consideration as being directed to a non-elected invention. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Appellants' claimed invention relates to the reduction of interference in integrated circuits. Appellants' technique uses fixed-value, nonprogrammable counters, rather than programmable counters, and clocks at least one of the counters at a slower rate. According to Appellants, the digital current in one part of an integrated circuit, which causes spurious tones in another part of the integrated circuit, is reduced using the disclosed technique. (Figure 4 and Spec. 14:13-15:23).

Claim 1 is illustrative of the invention and reads as follows:

1. A method of reducing interference in a circuit having a PLL, wherein the circuit is formed on an integrated circuit, the method comprising the steps of:

providing a divider circuit at the input of the PLL for dividing the frequency of an input signal by a desired amount; and

wherein the divider circuit is provided by placing first and second fixed-value dividers connected in series at the input of the PLL, wherein the first and second fixed-value dividers are configured to divide by respective first and second fixed non-programmable division factors.

The Examiner relies on the following prior art references to show unpatentability:

Bradley	US 6,087,865	Jul. 11, 2000
Dufour	US 6,111,470	Aug. 29, 2000

Claims 1, 3, 4, 52-54, 66-79, and 81-85, all of the appealed claims stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bradley in view of Dufour.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Brief and Answer for the respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Brief have not been considered and are deemed to be waived [see 37 C.F.R. § 41.37(c)(1)(vii)].

ISSUES

Under 35 U.S.C. § 103(a), with respect to appealed claims 1, 3, 4, 52-54, 66-79, and 81-85, would one of ordinary skill in the art at the time of the invention have found it obvious to combine Bradley and Dufour to render the claimed invention unpatentable?

The pivotal issues before us are whether Appellants have demonstrated that the Examiner erred in (i) interpreting the frequency divider components 220 and 221 of Bradley as corresponding to the claimed fixed-value dividers, and (ii) determining the obviousness to the skilled artisan of applying the phase locked loop (PLL) integrated circuit structure teachings of Dufour to Bradley.

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence:

1. Bradley discloses a programmable frequency divider which is an improvement over a prior art programmable frequency divider which utilizes a plurality of fixed divide-by-two frequency dividers. (Bradley, col. 1, ll. 28-40 and Figure 1).

2. Bradley's described improvement over the disclosed prior art frequency divider occupies less circuit board space and includes a mixer, a first input coupled to a reference oscillator and a second input coupled to a reference oscillator through a frequency synthesizer. (Bradley, col. 3, ll. 5-14).

3. In an embodiment of the programmable frequency divider illustrated in Figure 5, Bradley discloses (col. 6, ll. 42-65) the inclusion of series connected frequency divider elements 220 and 221coupled to a phase detector 213 which in turn is coupled to a voltage controlled oscillator (VCO) 210.

4. Bradley also discloses (col. 7, ll. 18-23) that the division factors Q and R of the frequency dividers 221 and 220 are selectable by a user to produce the desired output F_s.

5. Dufour discloses that a phase locked loop (PLL) frequency synthesizer including dividers, a phase comparator, and a voltage controlled oscillator (VCO) can be implemented in integrated circuit form. (Dufour, Figure 1 and col. 1, ll. 21-25).

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). "[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). Furthermore,

> "there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" . . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1741 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

ANALYSIS

Claims 1, 3, 4, 66-79, and 81-85

With respect to the Examiner's obviousness rejection of independent claims 1, 66, 77, and 85 based on the combination of Bradley and Dufour, Appellants' arguments in response assert a failure by the Examiner to establish a prima facie case of obviousness since all of the claimed limitations are not taught or suggested by the applied Bradley and Dufour references. Appellants' arguments focus on the alleged deficiency of Bradley in disclosing the claimed feature, present in each of the appealed

independent claims 1, 66, 77, and 85, of implementing a divider circuit by utilizing first and second fixed value non-programmable dividers in series. According to Appellants (Br. 13-15), the dividers 220 and 221 illustrated in Bradley's Figure 5 and described at column 7, lines 17-23 of Bradley are not fixed but, rather, are designed to be changeable according to a user's selection.

We do not find Appellants' argument to be persuasive in convincing us of any error in the Examiner's stated position. We agree with the Examiner (Ans. 7-8) that the series connected dividers 220 and 221 illustrated in Figure 5 of Bradley correspond to the dividers described and characterized by Appellants in their disclosure (Spec. 14:13-15:15 and Figures 4 and 26)) as being fixed-value non-programmable dividers.

It is apparent to us that the fact that the division factors R and Q in the respective dividers 220 and 221 of Bradley are selectable by a user can not be indicative of whether Bradley's dividers can be characterized as fixed value non-programmable dividers since the identified fixed value dividers 204 and 205 in Appellants' Figure 4 have division factors R1 and R2 which are also selectable by a user. In the example provided by Appellants (Spec. 15:3-8), with a reference frequency of 13 MHz and a desired divided signal output of 200 KHz, the values of R1 and R2 would be user selected to be 5 and 13, respectively, to provide the desired 200 KHz output (13 MHz ÷ 65 = 200 KHz).

With the above discussion in mind, we can only conclude, therefore, that the Examiner did not err in determining that Bradley's disclosed dividers 220 and 221 are indeed fixed value dividers, albeit after division

factor values have been user selected, precisely as what has been disclosed by Appellants. We also find it apparent that, similar to what is set forth in independent claim 85, the frequency divider 220 illustrated in Figure 5 of Bradley will be clocked at a lower frequency than the frequency divider 221 since the input to divider 220 is divided down by the division factor Q in divider 221.

We further find to be without merit Appellants' argument (Br. 13) which calls attention to the fact that the title of the cited Bradley patent is "*Programmable Frequency Divider*." We agree with the Examiner (Ans. 7) that, although the frequency divider 199 disclosed by Bradley may be described as a "programmable" frequency divider, it is apparent that such disclosed frequency divider has fixed value components such as the previously discussed dividers 220 and 221. It is further evident that Bradley's use of the term "programmable" does not mean that no fixed value components are used since the prior art frequency divider circuit 90 illustrated in Figure 1 of Bradley, which indisputably uses fixed value divide-by-two frequency dividers 110, is nonetheless described by Bradley (col. 1, ll. 29-31) as a "programmable frequency divider."

Lastly, we find to be unpersuasive Appellants' generalized statements (Br. 11-12) attacking the Examiner's basis for the proposed combination of Bradley with Dufour. We simply find no error in the Examiner's articulated line of reasoning (Ans. 5) which concludes that an ordinarily skilled artisan would have found it obvious to implement the phase locked loop (PLL) frequency divider circuitry of Bradley in integrated circuit form as taught by Dufour (Figure 1 and col. 1, ll. 21-25).

For the above reasons, since it is our opinion that the Examiner has established a prima facie case of obviousness which has not been overcome by any convincing arguments from Appellants, the Examiner's 35 U.S.C. § 103(a) rejection of independent claims 1, 66, 77, and 85, as well as dependent claims 3, 4, 67-76, 78, 79, and 81-84 not separately argued by Appellants, is sustained.

Claims 52-54

We also sustain the Examiner's obviousness rejection, based on the combination of Bradley and Dufour, of claims 52-54 which are directed to the reduction of interference near the output of voltage controlled oscillator (VCO) circuitry. We find no error in the Examiner's determination (Ans. 5) that the frequency divider circuitry of Bradley, which is designed to reduce harmonic interference (Figures 2A and 2B), would have reduced interference at the vicinity of the VCO circuitry 210 as a result of the frequency synthesizer circuitry 203 illustrated in Figures 4 and 5.

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that Appellants have not shown that the Examiner erred in rejecting appealed claims 1, 3, 4, 52-54, 66-79, and 81-85 for obviousness under 35 U.S.C. § 103.

DECISION

The Examiner's 35 U.S.C. § 103 rejection of claims 1, 3, 4, 52-54, 66-79, and 81-85, all of the appealed claims, is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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